GaN Essentials™

AN-013: Broadband Performance of GaN HEMTs

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2. Abstract

GaN devices offer significant improvements in broadband performance, resulting in design engineers increasingly turning to this technology for their next generation designs. This document discusses fundamental broadband design issues from both the theoretical and practical standpoints and compares GaN HEMT to GaAs FET and Si LDMOS technologies to show the advantages of each in broadband applications. A broadband GaN design example is presented to show results that can be expected from Nitronex's current generation of devices.

3. Broadband Matching Limitations

3.1. The Bode-Fano Limit

The Bode-Fano limit[1] describes the best theoretical match that can be achieved across a bandwidth to a load using a lossless network as shown in Figure 1. The Bode-Fano equation is expressed in Equation 1 and rearranged in Equations 2 and 3 in terms of maximum reflection coefficient and achievable bandwidth.

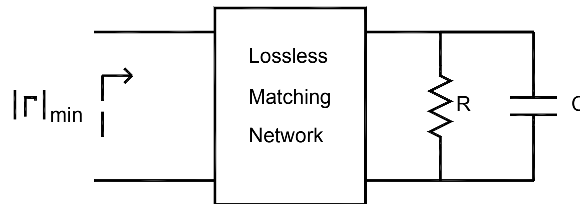


Figure 1. Network for which equation 1 applies

$$\int_0^{\infty} \ln\left(\frac{1}{|\Gamma|}\right) d\omega \le \frac{\pi}{RC} \tag{1}$$

$$\Delta f \le \frac{-1}{2RC\ln(|\Gamma|)} \tag{2}$$

$$|\Gamma|_{MIN} \ge e^{\frac{-1}{2\Delta fRC}} = e^{-\pi\frac{Q_2}{Q_1}} \tag{3}$$

$$\text{where} \quad Q_1 = \frac{R}{X_C} \quad and \quad Q_2 = \frac{f_o}{\Delta f} \tag{4}$$

In theory, for a purely resistive load (C=0), an infinite bandwidth matching circuit with no reflection loss could be constructed using an infinite number of lossless matching elements. Figure 2 illustrates this concept. As the number of matching elements is increased the reactance of each matching element is decreased, with the reactance of each element approaching zero in the limit. As the reactance of each element approaches zero the bandwidth approaches infinity. This concept can be applied to any impedance on the Smith chart, showing that you can match to the center of the chart without passing through a higher Q circle than the starting impedance point is on.

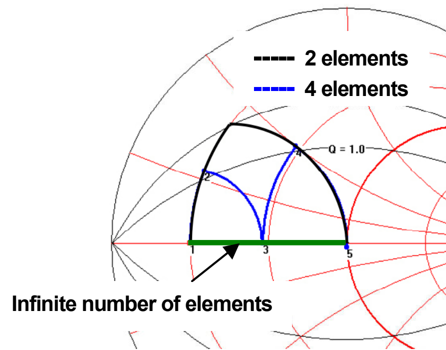


Figure 2. Graphical Illustration of the Bode-Fano Limit with C=0 Using Lumped Element Matching

Practical matching circuits often impose a far more reduced limit on achievable bandwidth. In these cases the Bode-Fano limit is of limited use as a measure of the goodness of a design, though it could potentially be used as a fundamental technology comparison.

3.2. Transformer Matching

At frequencies below approximately 600MHz transformers are common for broadband designs. These are well understood and are often used to match over 2 decades of bandwidth. Transformers can also provide a very high impedance transformation ratio, up to approximately 10:1 for 50-500MHz designs.

3.3. Quarter Wave Matching

Above approximately 500MHz transformer loss and bandwidth capability drop dramatically. Quarter wave transformers are commonly used in applications up to 3GHz and above. A practical quarter wave matching network of N sections is shown in Figure 3.

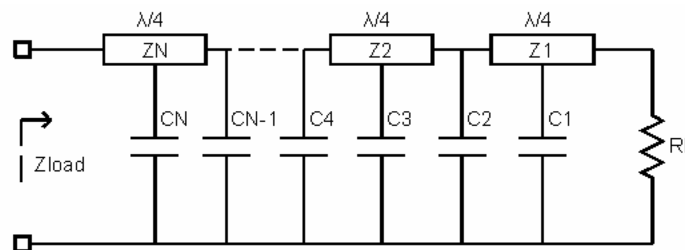


Figure 3. N-Section Quarter Wave Matching Circuit

The shunt capacitors between matching sections (C_2, C_4, … C_{N-1}) shift the impedance at that node roughly along the reactive circles on the Smith chart. The shunt capacitors in the middle of the sections (C_1, C_3, … C_N) shift the impedance roughly along the real axis of the Smith chart. The flexibility of a board using this layout can be very good and allow wide ranges of empirical tuning. Figures 4, 5, and 6 show normalized frequency responses of ideal Chebyshev (equal ripple) quarter wave transformers for various impedance ratios with maximum bandwidth at 10dB return loss. As a general rule of thumb for typical broadband designs 15dB return loss is excellent, 10dB return loss is good, 6dB return loss is about as poor as can be tolerated. With these rules of thumb and match return loss plots, an approximation can be made for performance across a given bandwidth for a given number of quarter wave matching sections.

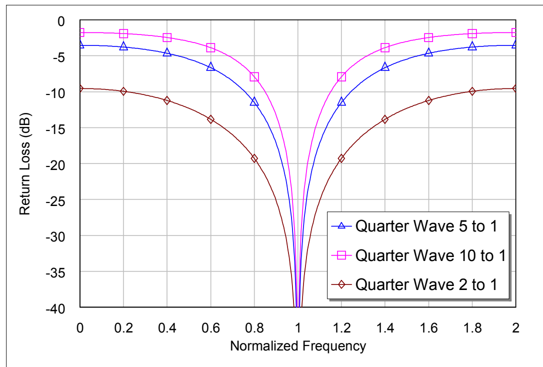


Figure 4. 1-Section ¼ Wave Match Return Loss

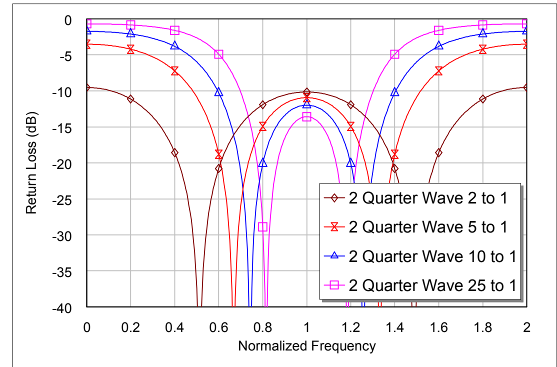


Figure 5. 2-Section ¼ Wave Match Return Loss

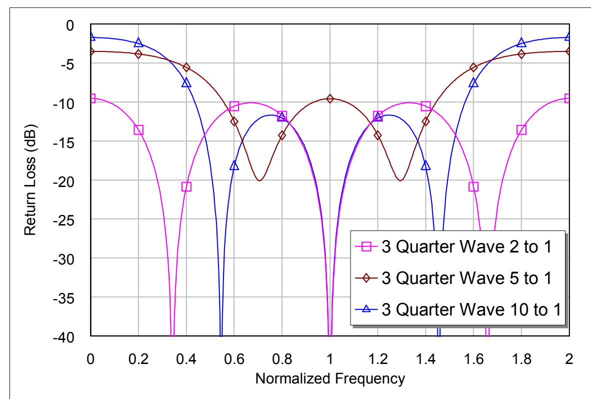


Figure 6. 3-Section ¼ Wave Match Return Loss

4. Broadband Design Methodology

As with most RF designs, there are many methodologies that can be used to realize a broadband design. A common and intuitive methodology employed by board level designers is discussed with examples to illustrate each concept. This paper focuses on the output network, which determines power and efficiency over frequency. The input matching network is typically more straightforward and primarily affects gain and return loss, and is not addressed in this paper.

4.1. Output Model Using Load-Pull Impedances

The first step in output matching network synthesis is to extract a model of the transistor output including package parasitics. One approach is to fit this model using optimum load-pull impedances. The model in Figure 7 would be fit such that the impedance looking into the drain with the source grounded matches the conjugate of the optimum load-pull impedances across frequency. The current source is shown for clarity but is omitted during modeling. For initial guesses for R_{DS} and C_{DS} use the guidelines in Section 5.1.

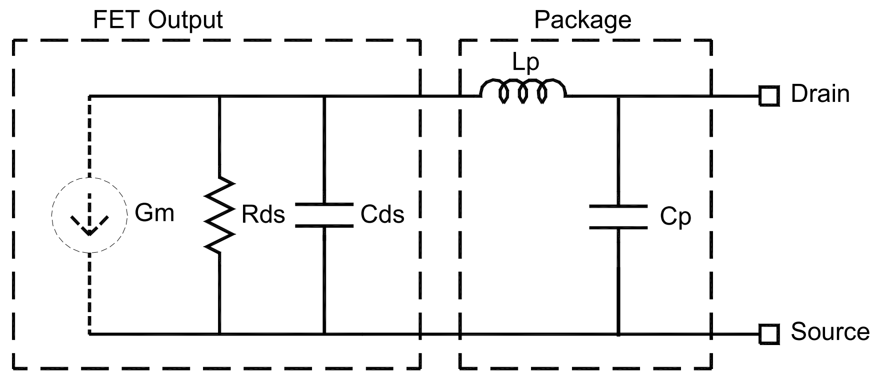


Figure 7. FET Output Model to be Fit to Conjugate Load-Pull Data

Modeled and measured conjugate load-pull impedances, along with model values, for the NPT25100 are shown in Figure 8. The FET values can be scaled linearly with power, and package parasitics can be scaled with package size using engineering judgment for an initial fitting value.

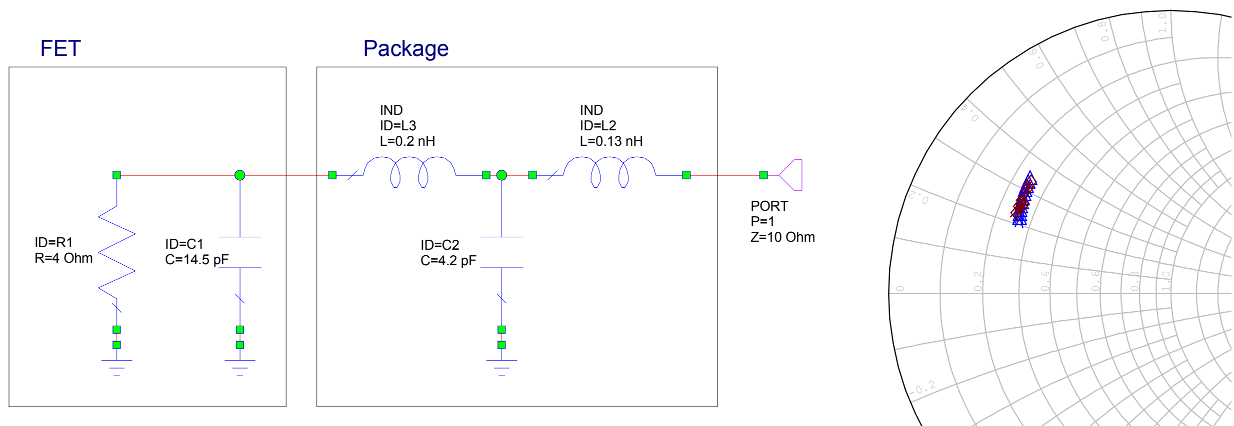


Figure 8. NPT25100 Model and Measured (Data Sheet) vs. Simulated Conjugate Load-Pull Impedances on a 10Ω Smith Chart from 2.14 to 2.7GHz

4.2. Matching Network Synthesis

The last step of the design is to synthesize a matching network. Using the model in Figure 8, an output match to 50Ω is synthesized to get the best return loss possible looking back into the network. The topology is chosen to trade-off complexity, size, loss, bandwidth, and other factors. As an example Figure 9 shows a 2 section quarter-wave transmission line match for the NPT25100 model shown in Figure 8. The load resistance is 4Ω giving a transformation ratio of ~12.5:1. Return loss of 10dB for this ratio is achieved across an octave of bandwidth, which agrees well with the curves shown in Figure 5.

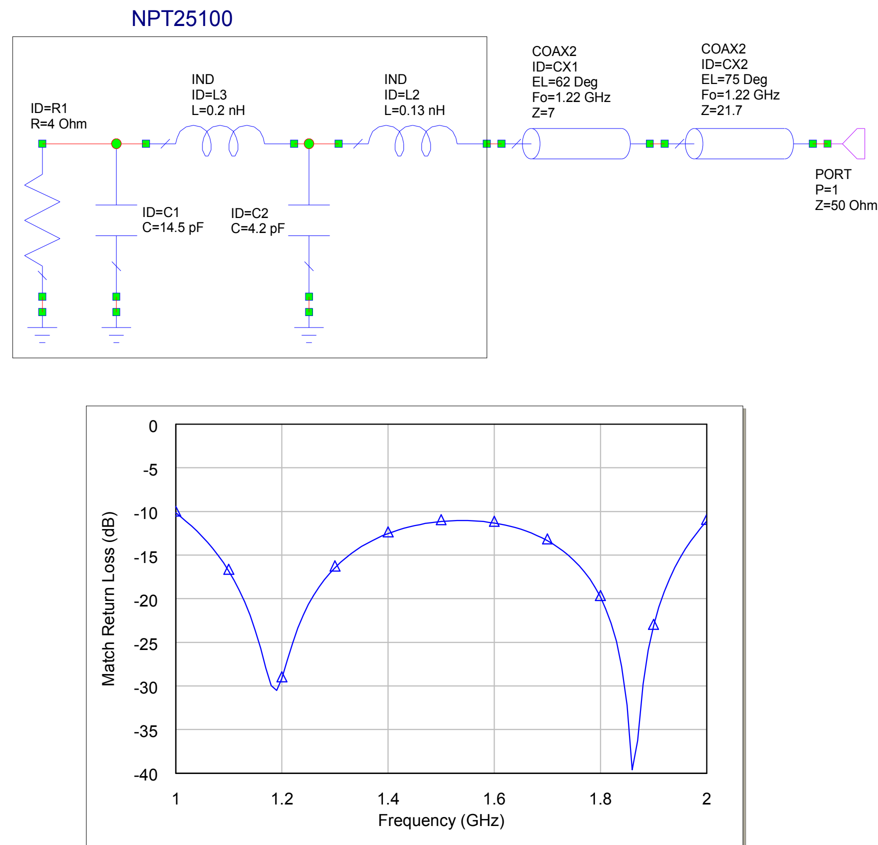


Figure 9. 1000-2000MHz NPT25100 Output Match Synthesized Using 2 Quarter Wave Sections

The quality of the return loss of this match is a critical figure of merit for how much inherent device performance is extracted in the design. At 15dB return loss, over 90% of device performance will be achieved across the band (a device capable of 100W at 65% efficiency will produce roughly 90W at 60% efficiency). More practical results are 8-12dB return loss with 6dB being the limit of what most designers would accept due to the efficiency reduction with so much power reflected.

5. GaN, GaAs, and LDMOS Compared

5.1. Bandwidth Limiting Factors

From the design methodology above it can be seen that there are 2 key parameters that determine performance across a given bandwidth: real impedance at the current source, and the Q of the parasitic components contained in the device. These properties can be used to compare the fundamental broadband capability of GaN, GaAs, and LDMOS technologies.

The real part, R_L, is primarily determined by the quiescent drain voltage of the device and can be estimated using basic load line theory by:

$$R_L \approx \frac{(V_{DD} - V_{knee})^2}{2} \Omega \cdot W \tag{4}$$

for a power match. An efficiency match will be slightly higher. For the NPT25100 R_L is $(28\text{-}4)^2/(2 \times 90W)$ = 3.2Ω which is a good approximation of the 4Ω modeled in Figure 8, which is a trade-off between power and efficiency.

The direct Q contribution from the FET is determined by C_{DS} as modeled in Figure 8. The package parasitics often degrade Q further. The lower the R_L the more Q is typically degraded, giving additional benefit to higher V_{DS} operation. For Nitronex NRF1 devices, C_O has been extracted to be approximately 0.15 - 0.2pF/W.

5.2. Limits to Unmatched Power in a Package

At low power levels and hence small FET sizes package parasitics are less significant. As power levels increase, the impedance of the power FET drops, reducing optimum load impedance and causing package parasitics to create high Q networks. Non-ideal matching losses also have a bigger negative impact at lower impedances, reducing achievable bandwidth. It becomes increasingly difficult to achieve broadband matching, particularly at frequencies above 1000MHz. This is the critical factor in determining how much broadband power can be achieved with a particular technology or device.

Consider two unmatched GaN HEMTs in a package: the NPT25100 with 90W narrowband saturated power, and a HEMT of two times that size. Models of each are shown in Figure 10. The 90W device model is from Figure 8, the 180W device uses values scaled from the 90W model. The smaller device, after package parasitics, has an output impedance conjugate of 3.05 + j1.0, for an impedance transformation ratio of 16:1 and a Q of 0.33 at 1.5GHz. The larger device has an output impedance conjugate of 1.55 + j1.25 for an impedance transformation ration of 32:1 and a Q of 0.8 at 1.5GHz. Following the methodology in Section 4 results in the simulations shown in Figures 10 and 11. Bandwidth is reduced by about 12% using ideal components. In a practical circuit application closer to 25% reduction would be expected. This example shows that this technology is capable of 10dB return loss across an octave of bandwidth with a 100W class device.

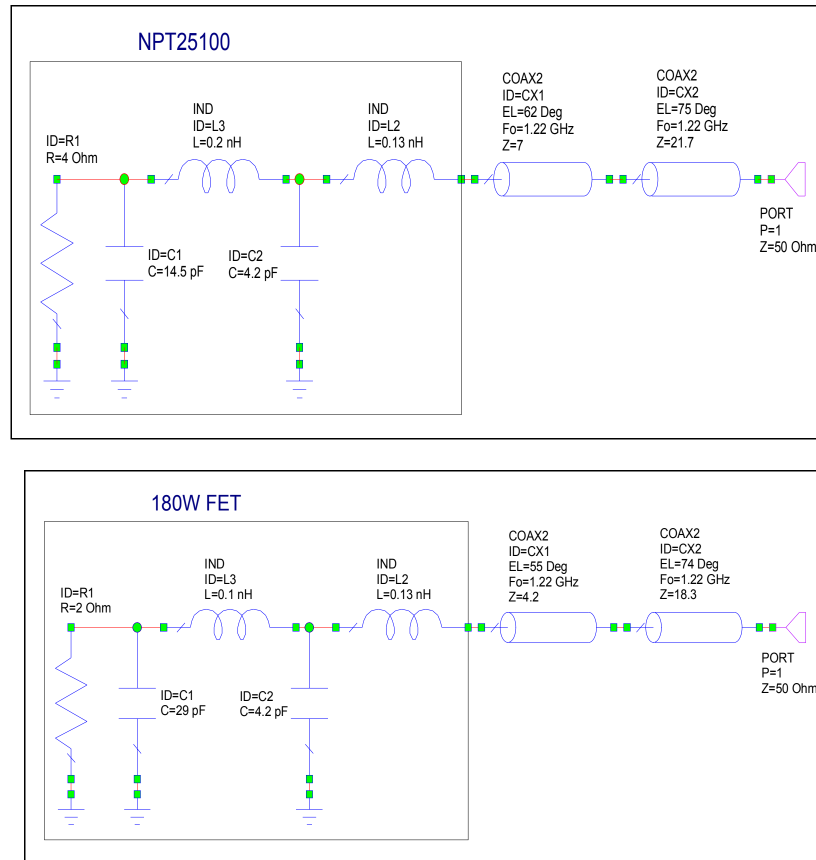


Figure 10. 90W and 180W GaN HEMTs Equivalent Output Circuit and Matching Network

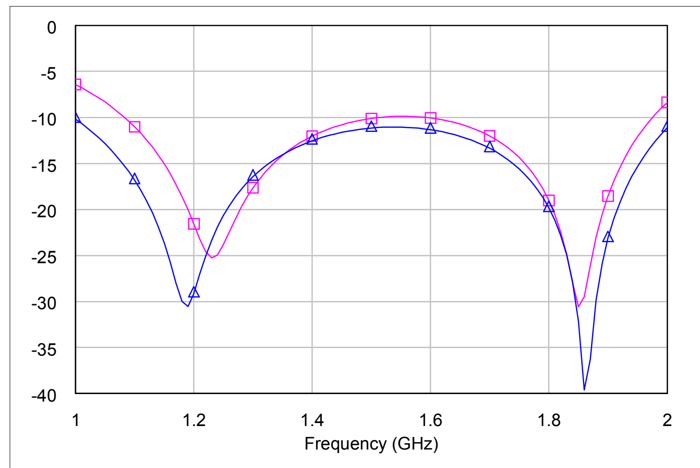


Figure 11. 90W and 180W GaN HEMTs Matching Network Return Loss

5.3. Die Level Technology Comparison

GaN HEMTs, GaAs pHEMTs, and Si LDMOS all have established positions in the broadband power amplifier application space. With any of these technologies the device manufacturer has many design variables that can affect performance dramatically. Among these are FET finger sizing and placement, epitaxial stack design, multi-die combining techniques, and packaging. From a fundamental technology perspective, it can generally be stated that for a given power level, GaN is able to provide wider bandwidths and higher peak DE than Si LDMOS. This performance advantage becomes even more pronounced at higher operating frequencies (e.g. >2.5 GHz). Key performance properties of the three major RF power transistor technologies derived from production ready products are shown in Table 1.

Table 1. Normalilzed Critical FET Parameters for 4 Production Released Devices

	Nitronex 5W GaN[2]	5W GaAs MESFET[3],[4],[5]	Nitronex 90W GaN[6]	125W Si LDMOS[7]
V_{DD}	28 V	28 V	28 V	28 V
FET Periphery	2 mm	4 mm	36 mm	180 mm(note 2)
Saturated Power	5.5 W	5.5 W	90 W	125 W
C_{LOAD}	0.17 pF/W	0.12-0.2 pF/W	0.17pF/W	0.48 pF/W
R_{LOAD}	360 Ω·W	225-250 Ω·W	360 Ω·W	Ω·W
$R_{TH,J-C}$(note 1)	117°C/W·W	179°C/W·W	157°C/W·W	55°C/W·W
Conj Z_{LOAD} Q (R+jX)	0.35 (58+j20) @ 900MHz	0.21 (41+j8.9) @ 900MHz	0.35 (3.6+j1.2) @ 900MHz	0.25 (1.48+j0.37) @ 900MHz

Note 1: $R_{TH, J-C}$ is specified in °C/W *P_{SAT} (W). To get the $R_{TH, J-C}$ of a given device, multiple the number in this row by the saturated output power of the device.
Note 2: 0.7W/mm assumed

Comparing GaN to GaAs in the 5W power level shows that both technologies have sufficiently low load impedance Q and similar impedance transformation ratios. Both technologies are using the same drain voltage and both have minimal contribution of parasitics to the load impedance. GaAs tends to have an advantage at higher frequencies as there are mature short gate length process nodes available. GaN has the advantages of improved thermal resistance and far higher output power capability.

Comparing GaN to Si LDMOS is more difficult. GaN has far higher power density which allows higher power levels to be put in a single packaged device. This reduces die-level parasitics and can allow for less complicated internal designs (smaller FET sizes) and therefore improved package parasitics and broader bandwidths. This results in a significant improvement in impedance transformation ratio (14:1 vs. 34:1), even at 900MHz. GaN is also a better high frequency technology and allows for higher frequency broadband designs to be realized. The lower power density of LDMOS has the advantage of inherently better thermal resistance. In some applications the power level achievable using GaN is limited by worst case junction temperature, therefore marginalizing the power density benefit.

It is easily seen that GaAs FET technology will be limited by thermal constraints. To develop a 100W power FET would require a die size not practical for commercial applications. GaAs has very good high frequency response and mature MMIC technology, having demonstrated 12 watts of RF power across 0.7-2.7 GHz[5]. Si LDMOS has had several generations of device development producing a good performance to cost trade-off, particularly for applications below 1500MHz. GaN HEMTs are unique in their ability to deliver higher power across broadband bandwidths than either GaAs FETs or Si LDMOS FETs. This is particularly noteworthy given GaN HEMTs are in their first generation of technology development. As upcoming generations further increase operating voltages, frequency ranges, and reduces thermal impedance and per unit capacitances, the performance gap for broadband matching will widen further.

6. Thermal Design

While the high power density of GaN has significant advantages from a broadband matching perspective due to reduced parasitics, it also leads to thermal challenges. Depending on the efficiency of a given design, heat dissipation may be the limiting factor in output power.

As an example, the NPT25100 has an R_{TH} = 1.75°C/W. The design example in Section 8.1 shows a design that achieves 50W output power at 50% drain efficiency. This gives a thermal rise of 87.5°C. A flange temperature of 85°C would give a junction temperature of 172.5°C, which would meet the requirements of most designers.

As another example, the NPTB00050 has an R_{TH} = 3.2°C/W. An octave bandwidth design from 1-2GHz with a matching topology that gives efficiency of 35% at 25W output power leads to a dissipated power of 46.4W and a thermal rise of 149°C. In this case output power must be reduced to meet thermal requirements.

A detailed discussion of board-level thermal design with Nitronex components can be found in the GaN Essentials Thermal Design document, available at www.nitronex.com. In general, broader band designs tend to yield lower efficiencies and therefore more dissipated power. Thermal design constraints should be checked early in the design to make sure they don't limit power too severely.

7. Robustness

Many broadband applications require the power device to be robust to very high VSWR loads without causing damage to the device. Nitronex devices have been tested in such environments and shown to have good robustness to being mistreated. Application Note AN-004, available at www.nitronex.com, shows the results of 10:1 and 20:1 output VSWR testing of the NPTB00050. Very small changes in output power and efficiency were noted after initial mismatch testing, and further testing showed no additional degradation.

8. Design Example

8.1. 500-1000MHz 50W PA Based on the Nitronex NPT25100

For this example, the goal was an octave bandwidth with 50W of output power. The design process was:

1. Determine output equivalent circuit
2. Synthesize output matching network
3. Small signal analysis using equivalent circuit and ideal matching network
4. Large signal model analysis
5. Final circuit design and layout

The output equivalent circuit was determined using the method shown in Section 4.1. Another technique is to directly fit the load-pull impedances with a matching network. The output equivalent circuit shown in Figure 8 for the NPT2100 was used for this design.

The second step, output matching network synthesis, was done using the method described in Section 4.2. Two cascaded quarter wave transformers were used, with impedance values determined by standard binomial filter tables.

Small signal analysis was used to check the design and showed good response. The NPT25100 model was developed primarily for power applications in the 2.5GHz range and is therefore not highly accurate over the 500-1000MHz range. Large signal simulations were used, however, to check trends and look for any changes in the simulation as non-ideal components were factored into the final schematic and layout. Initial and final simulations showed 50W across the band with worst case compression of 1dB at 750MHz.

The final circuit schematic is shown in Figure 12 with the output match response shown in Figure 13. A 3" x 5" Rogers 4350 board was fabricated with the layout shown in Figure 14. Figures 15 through 18 show measured results from the fully optimized evaluation board.

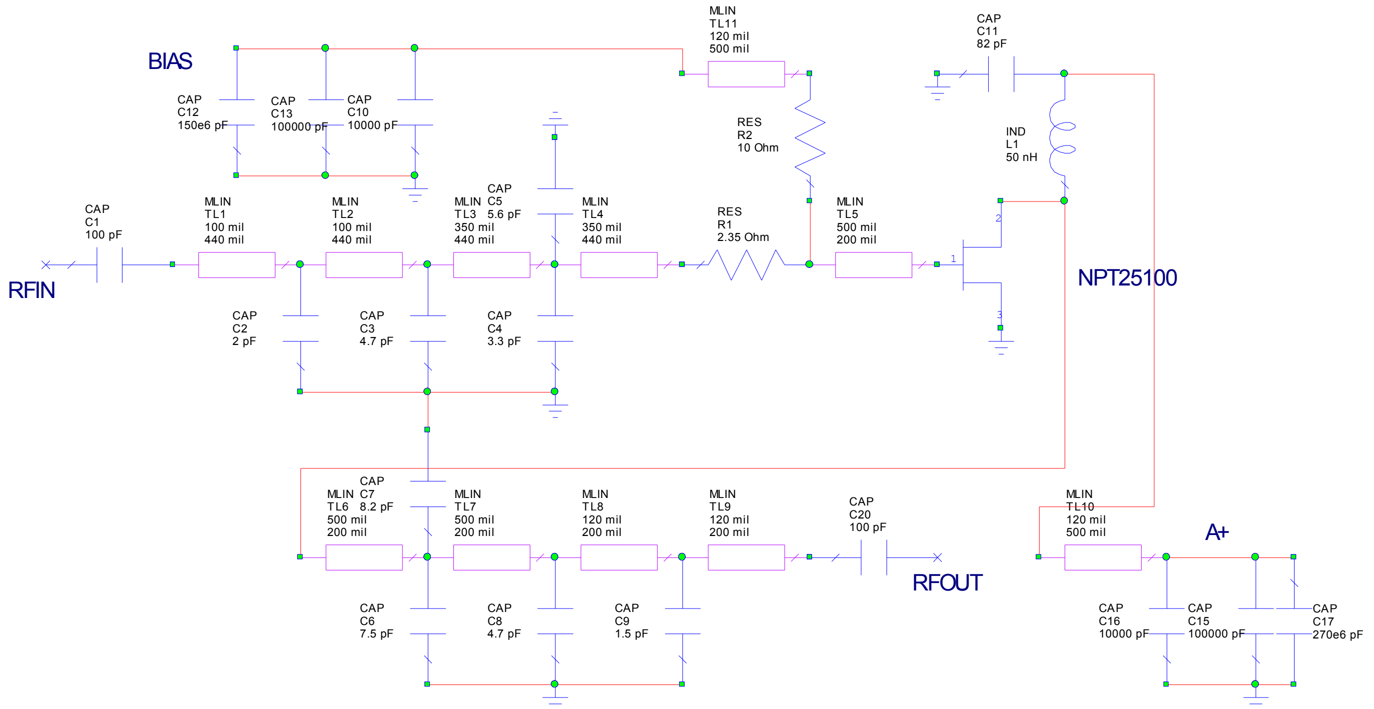


Figure 12. 500-1000MHz GaN Power Amplifier Schematic

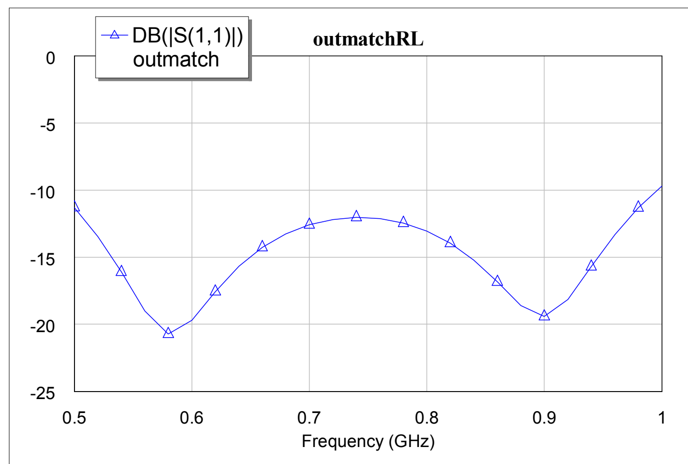


Figure 13. Return Loss of Output Match Looking back into Ideal Network and Device Equivalent Circuit

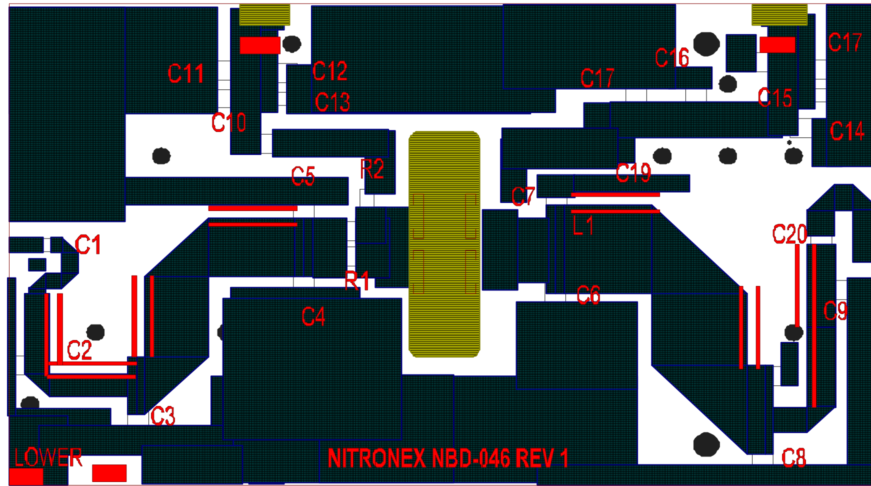


Figure 14. 500-1000MHz GaN Power Amplifier PCB Layout

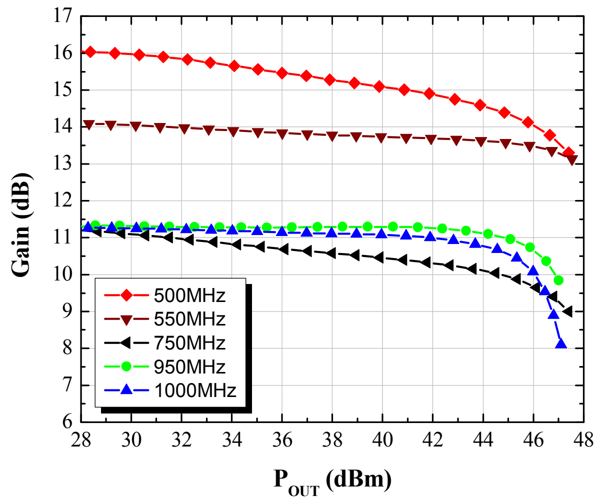


Figure 15. Gain Response across Frequency (V_{DS}=28V, I_{DQ}=700mA)

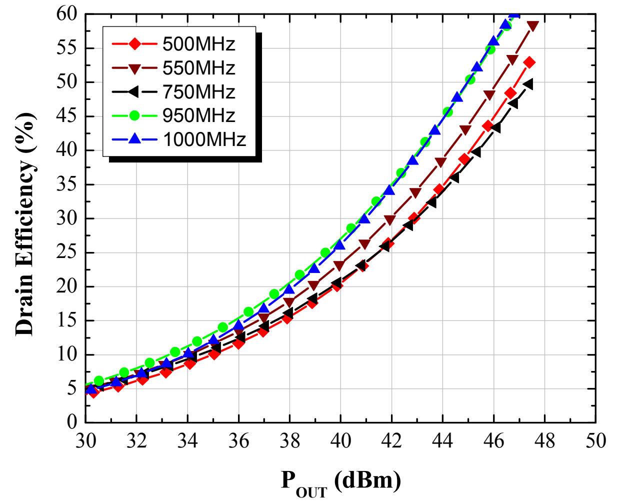
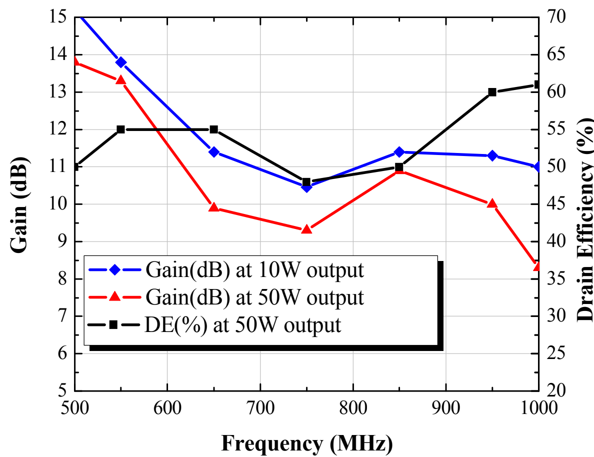


Figure 16. Efficiency Response across Frequency (V_{DS}=28V, I_{DQ}=700mA)



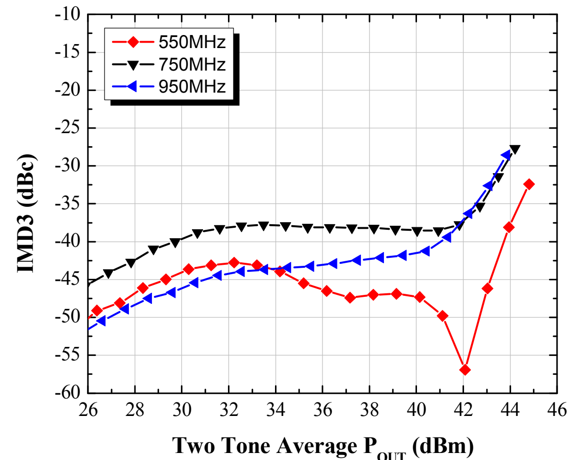


Figure 17. Gain and Efficiency across Frequency, P_{OUT}=50W (V_{DS}=28V, I_{DQ}=700mA)

Figure 18. IMD3 Response across Frequency (V_{DS}=28V, I_{DQ}=700mA)

9. Conclusions

GaN has a unique combination of high operating voltage and high power density, allowing broadband band high power designs than either GaAs FETs or Si LDMOS FETs. This is particularly interesting since current GaN HEMTs are first generation devices while both GaAs and Si are relatively mature technologies. The ability to develop higher power wideband designs with improved inherent robustness will continue to push GaN into an increasing number of applications. Future device generations will continue to widen this gap, making GaN an excellent fit for today's broadband designs.

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