

GaN Essentials™



AN-009: Bias Sequencing and Temperature Compensation for GaN HEMTs

GaN Essentials: Bias Sequencing and Temperature Compensation of GaN HEMTs

1. Table of Contents

1.	TABLE OF CONTENTS.....	2
2.	ABSTRACT	3
3.	BIAS SEQUENCING	3
	3.1. BIAS SEQUENCING.....	3
	3.2. GATE POWER SUPPLY NEEDS.....	4
4.	TEMPERATURE COMPENSATION	5
5.	CONCLUSION.....	9

2. Abstract

This application note will discuss fundamental usage methodologies to design with GaN HEMT devices. Specifically, this discussion will center on proper biasing techniques as well as temperature compensation surrounding GaN HEMT technology. A bias sequencing circuit and a temperature compensation circuit will be presented.

The biasing of high power RF devices, especially GaN devices, requires special attention. The concerns are mainly for preventing instabilities or oscillations, maintaining large drain current with a small voltage drop, and bias decoupling circuits to reduce interference with the RF matching circuit as well as limiting its influence on the linearity of the device. Also, properly maintaining the device current over temperature improves the performance in multiple operating environments. This application note will address the issues associated with biasing, bias sequencing and temperature compensation of a Nitronex GaN HEMT.

3. Bias Sequencing

GaN HEMTs are depletion mode devices which require a negative voltage applied to the gate. Supplying a negative voltage on a lab bench is easily accomplished by either using a supply with negative voltage generation capability or by switching the leads between the ground node and the positive voltage node. In a typical application circuit the negative voltage comes from a regulator or a negative voltage generator.

3.1. Bias Sequencing

For GaN HEMT devices, the first and most important issue is the biasing sequence. The goal while biasing the device is to stay away from areas which are sensitive to the potential instability of the device, for instance, the area where V_{DS} is low and I_{DS} is high. Assuming that the device is properly connected to a regulated power supply and that the drain and the gate are sufficiently DC decoupled and connected to 50 ohm terminations, the recommended bias sequence is as follows:

- Set $V_{GS} = 0V$ (gate), and $V_{DS} = 0V$ (drain).
- Decrease V_{GS} to beyond the Pinch-off voltage (V_P), typically -1.8 to $-2.2V$ for Nitronex's GaN devices.
- Increase V_{DS} up to the nominal voltage.
- Increase V_{GS} until the required quiescent current is reached.
- Apply the RF power.

Similarly, the recommended turn-off sequence is as follows:

- Turn off the RF power.
- Decrease V_{GS} down to V_P .
- Decrease V_{DS} down to $0V$.
- Set V_{GS} to $0V$

3.2. Gate Power Supply Needs

One needs to pay attention to how to deal with a positive gate current which will arise when the device is driven into saturation. Many commercial power supplies are not able to source and sink DC current through the same connector. One way to overcome this limitation is to use a resistor connected across the power supply terminals, this resistor will enable the power supply to always provide a negative current while allowing the device to source or sink current. The maximum value for this resistor is determined by the gate voltage and the amount of gate current required by the device. This can be calculated by the following:

$$R_{MAX} = \frac{-V_{GS_{MAX}}}{I_{GS_{MAX}}}$$

A 90W Nitronex device has nominal V_{GSQ} between -1.4V and -1.8V, and an $I_{GS_{MAX}} = 36\text{mA}$ (1mA/mm).

Moreover, the resistor's power rating also needs to be considered when selecting a gate resistor. For instance, with $V_{GSQ, MIN} = -2\text{ V}$, and 40 mA current a 50 Ohm gate resistor dissipates 0.08 W; therefore a 0.10 W resistor can be safely used.

Table 1. Quiescent and Saturated Gate Current vs Device Periphery

Nitronex Device	Device Periphery (mm of gate width)	$I_{GS,MAX}$ (mA) (Recommended Operating)	$I_{GS,MAX}$ (mA) (Absolute Maximum)	Recommended Resistor Value R_G (ohm)
NPTB00004	2	2	10	200
NPTB00025	8	8	40	50
NPTB00050	16	16	80	25
NPT25100	36	36	180	10

A series resistor (R_G) along the gate feed line is required to suppress oscillations; its value should be properly selected to keep the device stable as well as to limit the V_{GS} variation at the device versus the RF drive level. Table 1 lists the recommended minimum R_G for different devices based upon stability considerations. However, because the GaN HEMT's gate terminal is a Schottky diode its current draw will vary with RF drive level; at low drive levels the I_{GS} will be negative and in the mA range but as the device is driven into saturation I_{GS} will change polarity and increase to a maximum value of tens of mA's; see Table 1 for specific details. This change in I_{GS} will result in a voltage drop across the series gate resistor and a change in V_{GS} . To limit V_{GS} variation the gate resistor should not be too large; therefore the R_G values listed in Table 1 will be selected as the recommended values. The change in V_{GS} during device operation is therefore given by;

$$\Delta V_{GS} = R_G \Delta I_{GS} = -0.40V$$

It is interesting to note that V_{GS} will decrease (become more negative) as the device is driven into saturation such that the device will be pushed further into a pinch-off state when I_{GS} changes polarity.

Lumped capacitors can be used for DC blocking for applications at S Band and below to isolate the source and load from V_{GS} and V_{DS} . DC blocking capacitors are selected to have the series resonant frequencies in the band of interest to achieve low impedance as much as possible for these capacitors. They are also selected to have high Q so as to minimize insertion loss. The breakdown voltage of the DC blocking capacitors needs to cover the maximum voltage (DC + RF) they will be subjected to plus a little safety margin.

The drain bias line design criteria used for other high power RF devices can also be applied to GaN transistors. In order to accommodate high drain current and to achieve a low inductance a wide microstrip feed line is recommended. This will provide low power loss along the line as well as be a good starting point to providing adequate video bandwidth. The standard complement of bias line decoupling techniques can also be applied to GaN transistors.

4. Temperature Compensation

After making sure that the device is biased and operational, proper care must be taken to adequately maintain the bias of the device for consistent performance over temperature. The quiescent current of a GaN HEMT device is primarily a function of temperature and V_{GS} . Maintaining consistent performance can be accomplished by designing a bias circuit around the device so as to maintain a constant I_{DSQ} . As the graph shows below, V_{GS} changes proportionally to I_{DS} and temperature. For instance, a typical 90W GaN HEMT device, the NPT25100, needs $V_{GS} = -1.59V$ at a $-40C$ base plate, and $V_{GS} = -1.46V$ at a $+85 C$ baseplate to maintain $I_{DSQ} = 700$ mA.

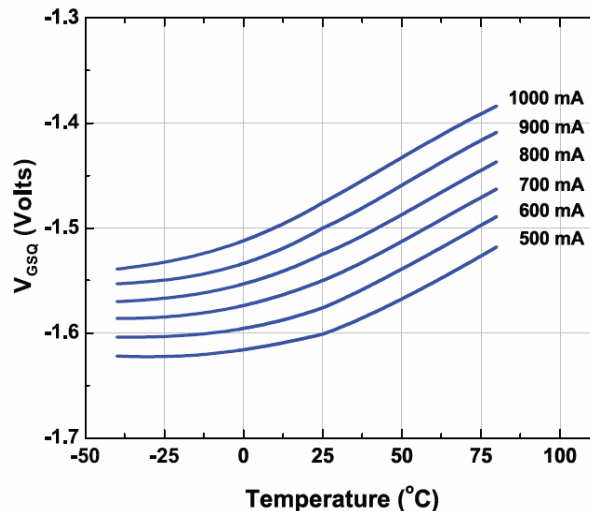


Figure 1. NPT25100 Quiescent Gate Voltage Required to Reach I_{DQ} as a function of Case Temperature

Given the above curves, a circuit needs to be developed to follow this shape as closely as possible in order to maintain constant I_{DSQ} . One such implementation for bias sequencing and gate bias control was built and tested and is shown in figure 2. The details of the design will be described in the sections to follow.

This circuit of figure 2 supplies a temperature compensated voltage to the gate to maintain a constant drain current. This circuit also includes the proper bias sequencing of gate and drain power supplies to operate the GaN device within a safe operating region to keep from damaging the device. The negative gate voltage is generated within the MAX881R bias sequencer so the gate bias network functions off a single +5V supply.

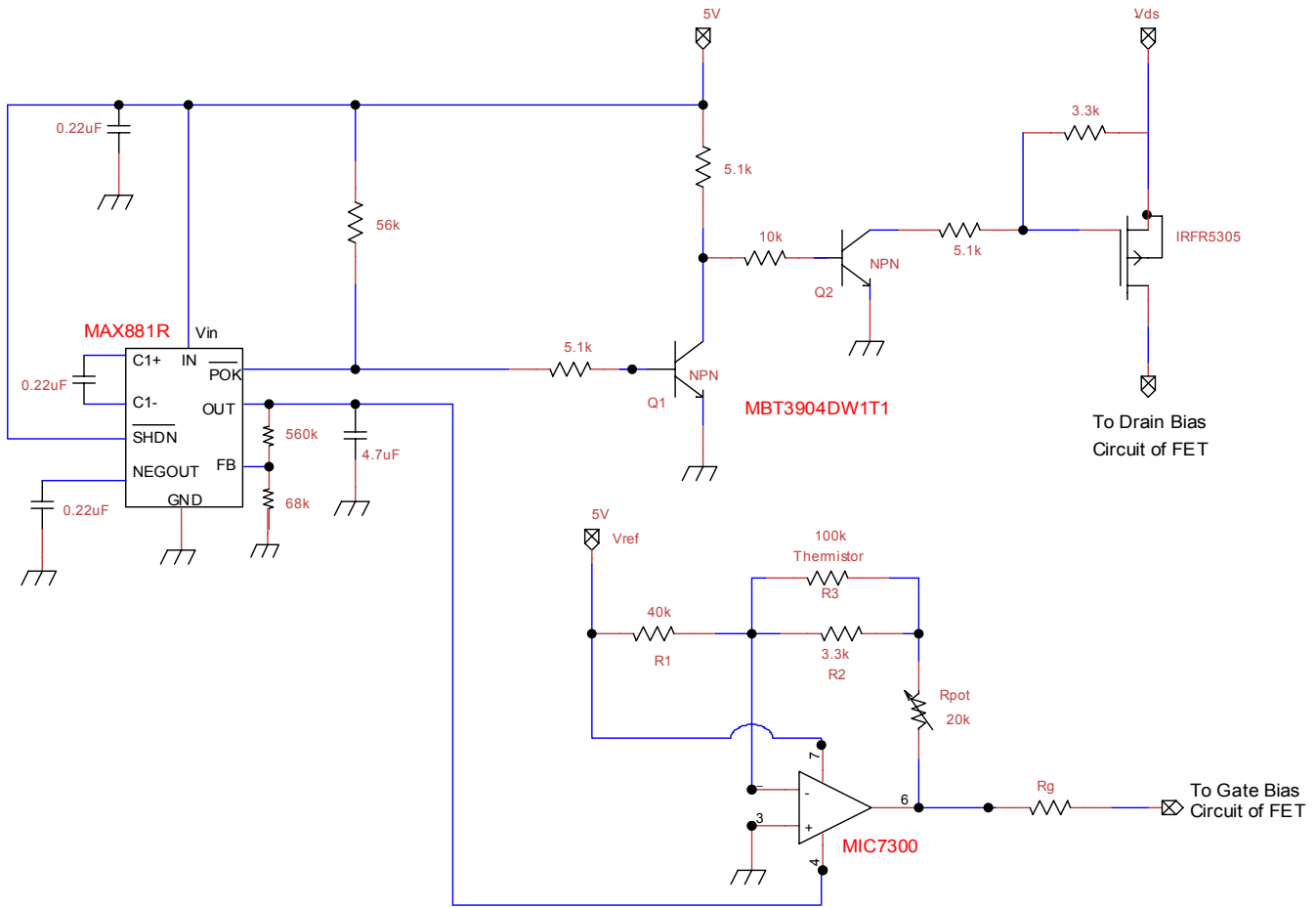


Figure 2. Recommended Bias Circuit for Temperature Compensation and Bias Sequencing

Table 2. Bill of Materials for Temperature Compensation and Bias Sequencing Circuit

Part Number	Description	Vendor
MAX881R	Bias Sequencer	Maxim
MIC7300	Operational Amplifier	Micrel
MBT3904DW1T1	Dual NPN	ON Semi
IRFR5305	HEXFET MOSFET	International Rectifier
ERT-J1VV104J	100k ohm 5%, 0603 Thermistor	Panasonic
3224W-1-203E	20k ohm Potentiometer	Bournes
Resistors	0603, 1%, Thin Film	Panasonic
Capacitors	0603, 10%, Ceramic	TDK

The circuit in Figure 2 uses a P-channel MOSFET as a high-side switch to deliver V_{DS} to the GaN HEMT. It is important to properly size this FET relative to the size of the HEMT being biased, in terms of $R_{DS(ON)}$, R_{TH} , and V_{DSMAX} . In general, smaller gate periphery HEMTs can be switched with smaller- and less expensive – MOSFETs. Specifically, $R_{DS(ON)}$ is selected to keep the voltage drop across the switch for a given maximum I_{DS} below a user-selected tolerance value:

$$R_{DS(ON)} < \frac{V_{drop}}{I_{DS\ max}}$$

Of course, V_{DSMAX} must exceed the maximum switched drain supply voltage with margin. And finally the MOSFET should have an R_{TH} which ensures that its maximum junction temperature is not exceeded even when the HEMT is drawing its maximum current (and the MOSFET is experiencing maximum power dissipation). As examples, a small 2mm HEMT may be safely switched with a small, inexpensive MOSFET with $R_{DS(ON)}$ as high as 500 milliohms in a SOT223-4 package. Larger 8mm and 16mm devices should use MOSFETs which keep $R_{DS(ON)}$ below about 150 milliohms and be housed in a DPAK or similar package with sufficient heat sinking. Even larger 36mm devices require switches with sub-80 milliohm $R_{DS(ON)}$ and packaging that will dissipate several watts.

The above circuit utilizes the international rectifier IRFR5305 MOSFET for the drain switch which has an $R_{DS(ON)}=0.065$ ohms and a V_{DSS} of -55V. Since the NPT25100 can draw 6 amps of RMS drain current the maximum voltage drop across the MOSFET is 0.39V and will dissipate 2.34W of power.

The bias sequencer and negative voltage is generated via the Maxim MAX881R bias supply IC which contains an integrated charge pump to supply the necessary negative voltage rail to the operational amplifier (assuming that a suitable system negative voltage is not already available) and generates a power-ok signal used to turn on the drain switch after the negative supply is stable. The operational amplifier must be capable of supplying the maximum negative and positive gate current for the HEMT being biased, and the charge pump must be capable of supplying the maximum negative current needed for that circuit. The Micrel MIC7300 operational amplifier can source or sink up to 80mA of current into large capacitive loads.

The V_{GSQ} and temperature compensated gate voltage is provided via the operational amplifier. The V_{GSQ} is set via the potentiometer (Rpot) and the op-amp circuit will maintain the proper I_{DQ} over temperature. The op-amp is configured as an inverting amplifier with the positive terminal grounded while the negative terminal is fed from a +5V voltage reference and a feedback circuit. The feedback circuit was designed to provide a temperature dependent voltage which tracks the actual device V_{GS} required to maintain a constant drain current. In order to implement the voltage tracking a thermistor is used in the feedback network. The thermistor (R3) provides a temperature dependent resistance and with the proper selection of other resistors a circuit can be designed which will accurately track the temperature dependent V_{GSQ} of the GaN device. The thermistor must be mounted near the active GaN device so as to measure the baseplate temperature of the device and as the thermistor resistance changes, the transfer function and therefore the output voltage of the op-amp circuit is modified so as to maintain a near constant I_{DSQ} versus temperature.

The transfer function of the operational amplifier is given by the following equations:

$$V_0 = -\frac{V_{ref}}{R1} \left(R_{pot} + \frac{(R2 + R3)}{R2R3} \right)$$

$$V_{GSQ} = V_0 - I_g R_g$$

Under non-saturated conditions the gate current will be in the mA range so the voltage drop across the gate resistor will be in the tens of mV range.

Using the spreadsheet located on the GaN Essentials webpage, the values of resistors in the temperature compensation circuit can be determined for a particular V_{GSQ} at 25°C case temperature. (Click the link located at <http://www.nitronex.com/ganessentials.html> to open the file.). Table 3 lists some recommended resistor values for setting different V_{GSQ} levels from Class-AB operation (-1.6 V) through Class-C operation (-3 V). As evident from the above equation and from the table, Rpot is used to adjust the room temperature gate voltage.

Table 3. Resistor values for fixed V_{GSQ} at 25°C case temperature for the NPT25100

V_{GSQ} (V) at 25°C	R1(Ω)	R2(Ω)	Rpot(Ω)	Rg(Ω)
-1.6	40k	3.3k	9.5k	10
-1.8	40k	3.3k	11.2k	10
-2.5	40k	3.3k	16.8k	10
-3.0	40k	3.3k	21.0k	10

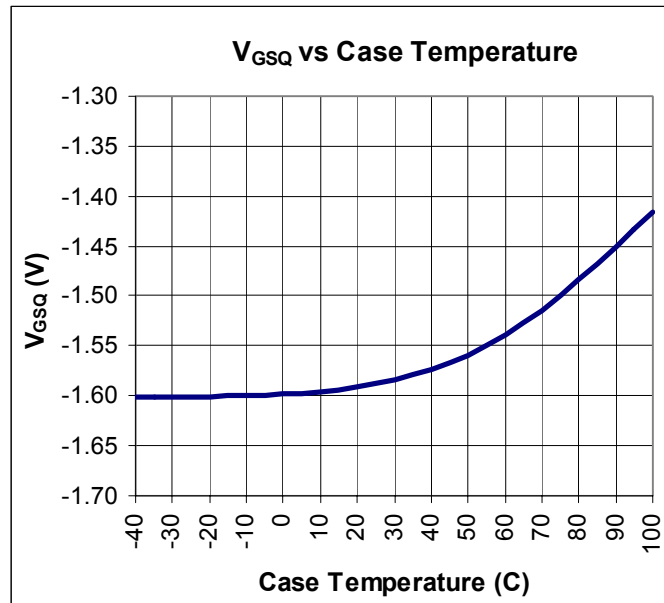


Figure 4. Modeled V_{GSQ} vs Case Temperature for Temperature Compensation Bias Circuit ($I_{DQ}=700mA$)

The graph in figure 4 was generated from the temperature dependent equation for V_{GSQ} , the shape of this curve tracks very closely with the actual NPT25100 device V_{GSQ} shown in figure 1.

5. Conclusion

In conclusion, this application note describes the proper bias sequencing necessary to safely turn on a GaN HEMT device and provides some discussion on selecting a gate resistor and operational details related to the gate terminal of the GaN HEMT. A bias sequencer and temperature compensation circuit was designed, built and tested. The schematic and BOM are provided so amplifier designers do not have to use valuable time in designing their own bias sequencer or temperature compensation circuit, others may wish to use this circuit as a starting point to create a different design.